



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Hirokazu HONDA

Confirmation No. 7187

Serial No. 09/678,609

Group 2827

Filed October 4, 2000

Examiner D. Graybill

MULTILAYER INTERCONNECTION BOARD, SEMICONDUCTOR DEVICE HAVING THE SAME, AND METHOD OF FORMING THE SAME AS WELL AS METHOD OF MOUNTING THE SEMICONDUCTOR CHIP ON THE INTERCONNECTION BOARD

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

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In compliance with Rules 1.97 and 1.98, and in ful-fillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed Form PTO-1449.

A concise explanation of the relevance of these items is that these references were cited by the Japanese Patent Office in an Official Action. A copy of the Japanese Official Action in which they were cited is attached hereto, with what is believed to be the pertinent portion enclosed in a wavy line. An English translation of the enclosed portion is also attached hereto.

Under the provisions of 37 CFR 1.97(e), the undersigned hereby certifies that each item of information contained in this Supplemental Information Disclosure Statement

HONDA S.N. 09/678,609

was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Statement.

Respectfully submitted,

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December 31, 2003

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Se several sheets if necessary)			Attorney Docket No.: 8013-11,47		Application No.: 09/678,609		
			Applicant: Hirokazu HONDA				
			Filing Date: October 4, 2000		Group Art Unit: 2827		
U.S. PATENT DOCUMENTS							
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^{*} Abstract provided for the Examiner's convenience